High Temperature Superconducting Space-Qualified Multiplexers and Delay Lines

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(Invited Paper)

Abstract— **A high temperature superconducting (HTS) four-channel multiplexer and a delay line were fabricated, space qualified and tested as part of the U. S. Navy's High Temperature Superconductivity Space Experiment II (HTSSE-II). The multiplexer had an architecture that included two branch-line hybrids and two identical parallel-coupled line filters per channel. Its operation was centered at 4 GHz, with 50-MHz-wide channels. It was fully integrated, with microstrip interconnections between channels and thin-film load terminations in the out-of-phase port of the output hybrid. The delay line was made up of two cascaded modules for a total delay of 45 ns between 2 and 6 GHz. Both devices were made using 5-cm-diameter $LaAlO_3$ wafers coated with epitaxial thin film $YBa_2Cu_3O_7$, on both sides in the case of the delay line. Both devices operated at 77 K.**

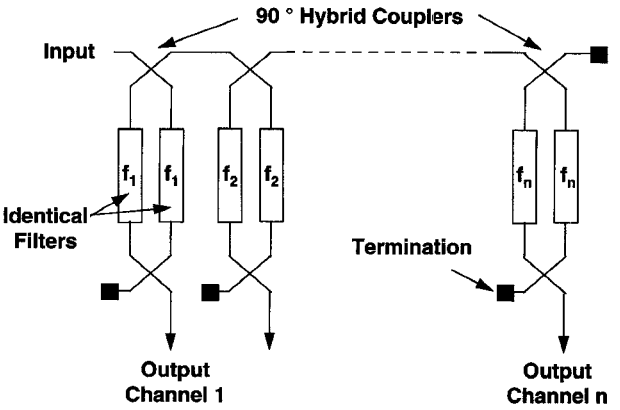

Fig. 1. HTS multiplexer architecture.

I. Introduction

MICROWAVE multiplexers and delay lines are of interest in communications as well as radar and electronic warfare (EW) systems. Some of these applications have insertion loss requirements that make the use of high temperature superconductors (HTS) an attractive alternative to much bulkier conventional technology, specially in space-borne systems, where weight and volume are very expensive.

The high temperature superconductivity space experiment II (HTSSE-II) will provide an excellent vehicle for testing the technology with a view to applications not only in space systems but others as well, which would benefit from the rigorous testing and manufacturing schedule imposed by the program.

In this paper we discuss our participation in HTSSE-II with two HTS microwave components: A four-channel bandpass multiplexer and a 45 ns delay line. The design characteristics of both devices are given in Table I. $YBa_2Cu_3O_7$ (YBCO) thin films deposited epitaxially by off-axis sputtering on single-crystal $LaAlO_3$ (LAO) substrates were used to fabricate the devices, intended for operation at 77 K.

Only a handful of groups have published work on HTS bandpass multiplexers. Fathy *et al.* discussed the multiplexing of HTS bandpass filters using ferrite circulators at cryogenic temperatures, but only included preliminary results in their paper [1]. The group lead by Mansour [2]–[5] have reported work on several types of multiplexers, including hardware delivered to the HTSSE-II program [5]. A comparison of conventional and HTS multiplexers is also given in [5].

Work on superconducting delay lines, on the other hand, started at Lincoln Laboratory well before the advent of high temperature superconductivity [6], and concentrated mostly on linearly dispersive delay lines for analog signal processing. Work on HTS nondispersive delay lines has taken place since [7]–[12], including two recent instantaneous frequency measurement subsystems based on banks of delay lines [9], [12]. A comparison between conventional and HTS nondispersive delay lines is given in [14].

Earlier accounts of the work to be presented here were given in [13] and [14]. In the present paper we elaborate on aspects related to the specific devices delivered to HTSSE-II and how we arrived at their final versions, including design, fabrication and test data not provided before.

II. Multiplexers

A. Design

The design goals for the four-channel multiplexer are listed in Table I. The multiplexing architecture chosen is shown in Fig. 1. It can accommodate as many channels as the bandwidth of the 90° hybrid coupler covers. Multiplexer architectures

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TABLE I
MULTIPLEXER AND DELAY LINE DESIGN CHARACTERISTICS

Multiplexer	
Architecture (each channel):	Two 90° hybrids and two filters
Configuration:	Microstrip
Filter type:	Chebychev
Filter order:	4
Maximum passband ripple:	0.1 dB
Ripple bandwidth:	50 MHz
Topology:	Parallel λ/4 coupled sections
Guard band:	16 MHz
90° Hybrid type:	Branch-line
Channel #	Center Frequency (MHz)
1	3901
2	3967
3	4033
4	4099
Delay Line	
Configuration	Stripline
Frequency Range	2 GHz - 6 GHz
Delay	> 40 ns
Insertion Loss	< 1 dB

based on one filter per channel are generally limited to a maximum of ten or twelve channels. The effect of multiplexing on the filter responses and the need to introduce guard bands between channels was discussed in [13]. A 16 MHz guard band was introduced in order to mitigate this effect.

The hybrid coupler used in this project was of the branch-line type. It is a 10% bandwidth coupler which sufficed to cover the four-channel bandwidth. More sophisticated coupler designs can be used for wider bandwidth coverage.

A four-pole quarter-wavelength parallel-coupled section microstrip topology with 500-μm-thick LAO was chosen for the channel filters. The filter structure and design parameters are shown schematically in Fig. 2. Because of the requirement to work at 4 GHz, which makes the filters relatively large, it was necessary to establish the practical constraint of having each filterbank channel fit on a 5-cm-diameter wafer. Other filter topologies or even thinner LAO substrate wafers could have been used to minimize the filter area. However, we adopted a conservative approach and chose the configuration in Fig. 2 based on previous experience [15], [16].

From calculated estimates of the insertion loss for the required 50 MHz bandwidth (1.25%) filter (see Fig. 3 in [13]),

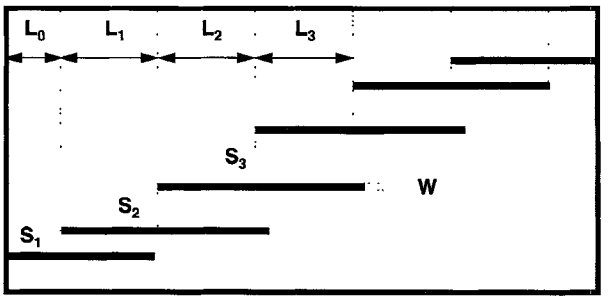


Fig. 2. HTS multiplexer filter topology.

it was decided that superconducting ground planes were not as critical as when working at higher frequencies. Hence, plated gold ground planes were used, with an insertion loss expected to be around 0.8 to 1 dB for YBCO films with R_s between 0.5 and 1.5 mΩ (at 10 GHz and 77 K).

A first, prototype version of the multiplexer was made prior to the final flight unit, to test our design and packaging concepts. The final version comprised a revision of the design and the overall fabrication and packaging approaches. The

TABLE II
MULTIPLEXER VERSION DIFFERENCES

	Preliminary	Final
Channel Interconnect	External	Internal (microstrip)
Terminations	External (coaxial)	Thin film (integrated)
Electrical Design	Circuit model software	Circuit model and EM field solver softwares
Package	All niobium	Niobium and aluminum
Device	Prototype	Qualification and Flight Units

TABLE III
LOOK-UP TABLE HTS FILTER DESIGN APPROACH

Step 1	Start with conventional approach design using circuit-model-based software
Step 2	Generate parallel coupled microstrip line Look-Up Table using EM field solver
Step 3	Interpolate table to obtain required coupling gap
Step 4	Analyze resulting filter using EM field solver
Step 5	Compute length correction for each section based on center frequency offset
Step 6	Iterate process. Go back to Step 4

TABLE IV
COMPARISON BETWEEN CONVENTIONAL AND LOOK-UP TABLE APPROACHES
$W = 0.176$ mm $L_1 \cong L_2 \cong L_3 \cong 4.788$ mm

Parameter	Required Coupling (dB)	Touchstone™ (mm)	Look-Up Table (mm)
S_1	-17.6	0.572	0.530
S_2	-35.8	2.367	1.931
S_3	-37.8	2.772	2.161

final filter design technique was developed based on iterations between conventional software tools, which use empirical models of microwave circuit elements, and an electromagnetic field solver. The differences between the preliminary and the final devices are listed in Table II.

The design for the preliminary version followed a conventional approach [15], [16]. The software Touchstone™ was used. As will be seen below, however, this yielded unsatisfactory results and a more sophisticated approach was developed, using the EM analysis software Sonnet™. This approach was based on the generation of a look-up table for the coupling parameters of edge-coupled lines [17]. The steps followed are summarized in Table III.

The conventional and the look-up table approaches resulted in substantially different filter dimensions as can be appreciated from Table IV, with reference to Fig. 2.

The reason for the discrepancy and for the inadequacy of the conventional design tools is that the range of validity of the empirical circuit models these tools are based on is rather limited. Thus, the LAO substrate relative dielectric constant of 23.4 is higher than the values most of these models can support. In addition, the coupling values required for narrow band HTS microstrip filters of the type discussed here are smaller than these models can support. Hence the increasing discrepancy between conventional and the more involved look-up table approaches as the required coupling decreases.

Thin film load terminations were used for the out-of-phase port of the output hybrid coupler in every channel of the final version of the multiplexer (see Fig. 1). These terminations followed a simple design based on a resistive thin film and a shunt capacitance to ground to resonate out the inductance in the resistor section [13].

B. Mask Layout and Wafer Fabrication

The mask layout for each channel of the preliminary version multiplexer included only the channel. As the fabrication process and its monitoring were better understood by the time

TABLE V
PROCESS SEQUENCE FOR FINAL VERSION OF HTS MULTIPLEXER
SUBSTRATE IS 5-CM-DIA., 500-μm-THICK $LaAlO_3$, WITH YBCO ON ONE SIDE

Mask	Description	Material	Thickness	Process
1	Contact to YBCO	Au	2000 Å	Lift-off
	Contact anneal	Au on YBCO	N/A	550°C
None	Ground plane base	Cr/Au	200/2000 Å	Sputter
	Ground plane thick metal	Au	2 μm	Electroplate
2	Filter	YBCO	4000 Å	Ion mill
3	Resistor	Mo/Ti	1140/100 Å	Lift-off
4	Capacitor and contact pads	Cr/Au	200/2000 Å	Lift-off

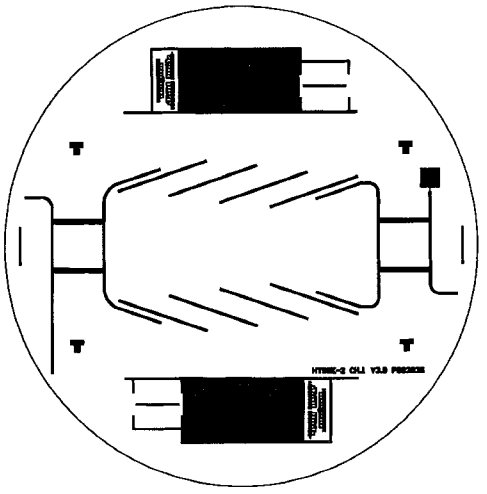


Fig. 3. Mask layout for channel 1 of the final HTS multiplexer. Mask includes microstrip transition chips for channel interconnection and post-processing test patterns.

the final version was designed, the corresponding mask layout, shown in Fig. 3, included several test patterns which allowed assessing and monitoring the YBCO quality during and after processing. The final version also had internal channel-to-channel interconnections and so the mask layout included microstrip line sections used for the connection.

The fabrication techniques used for the final device were more elaborate than for the preliminary one because of the integrated load terminations. However, the processing of wafers for the final version was more stable and reliable, as better techniques were developed for each of the fabrication steps needed.

The processing sequence used to fabricate the channels of the final version of the multiplexer comprised five major steps, requiring four mask levels, in addition to the step in which the filter chip is sawn from the wafer. The sequence is summarized in Table V. The fabrication steps followed for the preliminary version were a subset of those shown in Table V, since only YBCO patterning and annealed contact

TABLE VI
YBCO CHARACTERISTICS MEASURED AFTER PROCESSING

Wafer #	R_s (mΩ)* (10 GHz, 77K)	YBCO Sheet Resistance (300 K)(Ω/sq)	J_c (A/cm²)	T_c (K)
1	0.72	7.5	10^6	87
2	1.4	8.1	2.2×10^6	90.3
3	2.97	15.7	2.7×10^5	82
4	N/A	8.5	1.2×10^6	86.4

*Surface resistance measured with parallel plate resonator

definition were required. Therefore only the fabrication of the final version will be discussed in detail here.

The starting wafer was LAO, 5 cm in diameter and 500 μm thick, coated on one side with YBCO. Generally, the surface resistance of the YBCO film was measured at 77 K before processing was initiated to ensure that the starting film was of high quality. Au contacts were defined using lift-off (image-reversal lithography) of sputtered Au in the first mask level. The Au was then annealed into the YBCO at 55°C in a flowing-oxygen ambient. The ground plane was formed on the uncoated side of the substrate by sputtering Cr/Au (Cr promotes adherence between Au and LAO) and then plating an Au layer to adequate thickness (2 μm). The second mask level was required for patterning the YBCO film into the filter structure by argon ion milling. The 50-Ω resistors were defined by lift-off in the third mask level. The resistor material was Mo, with a Ti capping layer to protect the Mo from oxidation under ambient conditions. The capacitance structure, which acted as an RF short from the load resistor to the ground plane, was created in the final mask level. Contact pads for test patterns on the wafer were also formed in this step.

The test patterns on the wafer allowed post-processing measurements of T_c, J_c, and RF surface resistance of YBCO, Mo/Ti sheet resistance, and Au/YBCO contact resistance. In particular, the RF surface resistance was measured using a parallel-plate resonator technique [18]. Table VI shows the results of the post-processing measurements of the YBCO characteristics on four sample wafers. Table VII shows all

TABLE VII
ADDITIONAL WAFER CHARACTERISTICS MEASURED AFTER PROCESSING
(SEE TABLE VI FOR POST-PROCESSING YBCO CHARACTERISTICS)

Wafer #	Au/YBCO Contact Resistance[2] (77 K)(Ω/sq)	Mo/Ti Sheet Resistance (300 K)(Ω/sq)	Mo/Ti Sheet Resistance[1] (77 K)(Ω/sq)	Mo/Ti Sheet Resistance Ratio
1	10^{-6}	2.31	1.4	1.65
2	1.5×10^{-7}	2.69	1.85	1.45
3	7×10^{-5}	2.51	1.6	1.57
4	1.2×10^{-4}	3.02	2.12	1.43

Notes:
1. Mo/Ti sheet resistance target value was 1 Ω/sq. Variance not critical to filter performance.
2. Au/YBCO contact resistance correlates with substrate cleaning technique prior to Au sputtering: Wafers 1 and 2 were ion milled; Wafers 3 and 4 cleaned by back-sputtering.

other characteristics measured. Notice that there is good correlation between the measured superconducting properties of the YBCO film (R_s, T_c, and J_c) and the YBCO sheet resistance at room temperature. From these results a simple process monitoring technique was developed, using a four-point-probe measurement at room temperature as a valid check for the film quality at every step of the fabrication.

C. Packaging and Assembly

A major element of the packaging of the multiplexer and the delay lines was the need to house microwave circuitry fabricated on large area substrates. A significant milestone in this effort was the adoption of niobium as the thermal-expansion-matched carrier material for the LAO substrates. The LAO substrates were attached to the niobium carriers using thin indium sheets. Other important elements in the development of the packaging approach used were the adaptation of the gold plating technique used for stainless steel to niobium parts and the use of Wiltron K-connectors. Hermetic sealing was considered at first but was later dropped as a requirement when it became evident that good quality YBCO films do not degrade upon long exposure to even humid atmosphere.

Niobium was used for all package components in the preliminary version of the multiplexer. However, this resulted in a very heavy package which, nevertheless, demonstrated the viability of the entire concept under development. The niobium carrier-LAO substrate assembly was then attached to a niobium frame carrying the connectors by means of soldering with indium strips placed along ledges on the frame. All pieces were gold plated. The four-channel multiplexer consisted of four packages housing individual channels connected externally using semirigid coaxial cable. The entire assembly was then mounted on a copper plate for mechanical support and to facilitate cooling. The weight of the prototype device was 1.5 kg.

A significant improvement was added to the packaging of the flight device, however, by using aluminum as the major framework material for the package. Niobium carriers were still used to mount the patterned LAO substrates; however, the carrier-substrate assemblies were then mounted in an aluminum frame with the connectors by means of special springs attached to the frame. The springs accommodated the difference in thermal contraction between the niobium carriers and the aluminum frames. The use of springs also resulted in relaxed internal dimensional tolerances and made mounting and demounting the carrier-substrate assemblies much easier. Top and bottom package lids were also made in aluminum. Further lightening of the package was achieved by removing material from the underside of the carriers, leaving a ribbed pattern to maintain mechanical strength. The result was a significantly (64%) lighter package than the all-niobium prototype, and a much more versatile and reliable packaging technique.

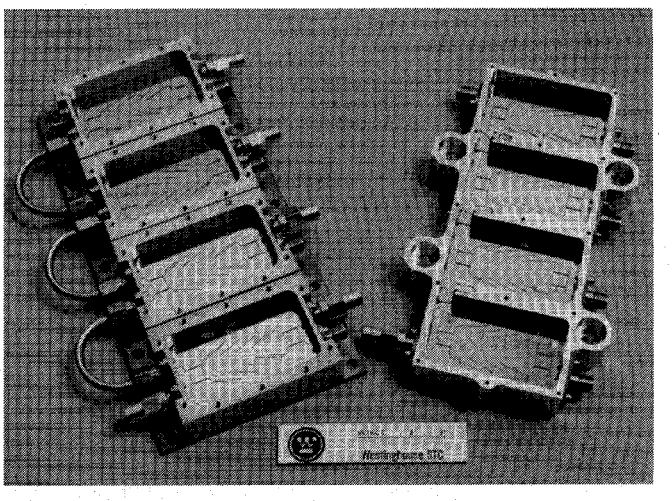


Fig. 4. Photograph of the prototype and final multiplexers.

The prototype multiplexer channels were made each with four external connections that allowed thorough testing before assembly into a multiplexer. Fig. 4 is a photograph where both the prototype and the final multiplexers are shown side by side for comparison. The external coaxial 50-Ω terminations and interconnections between channels and the mounting plate can also be seen. The package of the final unit delivered includes mounting holes required by the space system integrator. Short microstrip sections on individual substrate pieces, described in the previous section, were used as interconnections between channels in the final device. The mounting technique for these interconnect pieces was optimized in a separate dual-channel package. Fig. 5 is a close-up photograph of the interconnect, made up of a separate microstrip line section mounted between two channel sections. Gap-welded gold ribbon was used for these interconnections as well as for the contact between the coaxial connector center pin and the YBCO microstrip lines.

D. Experimental Results and Discussion

Fig. 6 shows a composite response for all four channels of the prototype multiplexer measured between 3.5 and 4.5 GHz at 77 K. The markers indicate the design goals for the center frequencies. The response of this prototype device was clean enough to show the viability of our overall approach. The deep notch on the lower skirt of the fourth channel is due to interaction with the previous channel; notice that the notch occurs in the center of the previous channel.

The measured responses for the channels in the final flight device were given in [13]. Fig. 7, the composite for all four

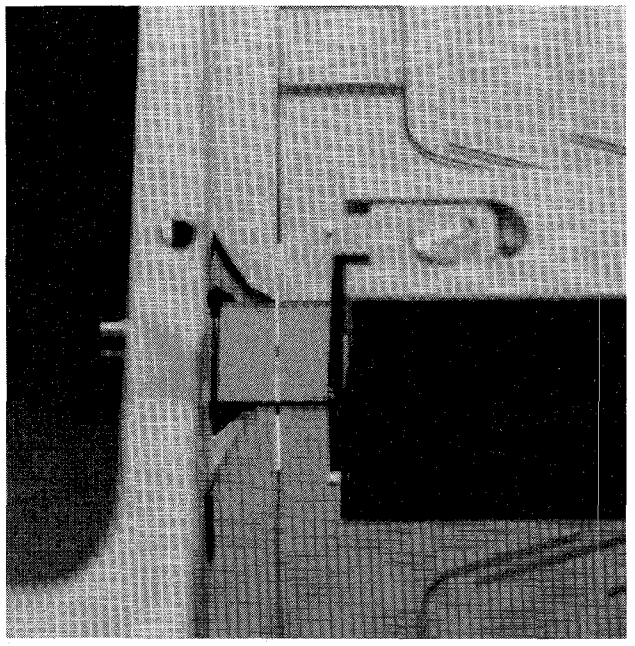


Fig. 5. Close-up photograph of the microstrip channel interconnection in the flight HTS multiplexer.

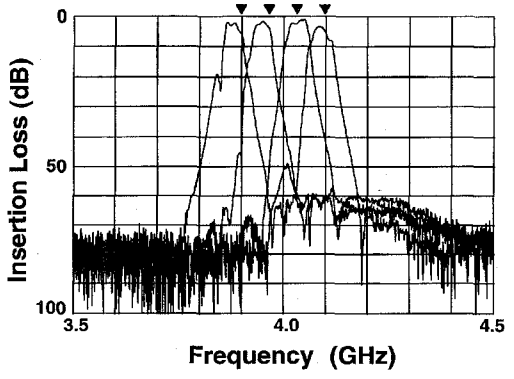


Fig. 6. Composite response of all four channels of the prototype multiplexer. The markers indicate the design center frequencies.

channels measured between 3.5 and 4.5 GHz at 77 K, is reproduced here for completeness. The notches on the lower skirts of channels 2–4 are due to the multiplexing effects discussed in [13]. The passbands are much cleaner and uniform than for the prototype device, and their shapes are much closer to the designed Chebychev response.

Fig. 8 shows the same composite response as in Fig. 7 but on an expanded vertical scale (2 dB/div). The markers are placed on the design goal center frequencies (see Table I). The insertion losses measured for all the channels is relatively high, around 2 dB, which is about 1 dB higher than expected from calculations of mid-band filter loss at 4 GHz using a gold ground plane (see Fig. 3 in [13]). Return loss data did not clearly shed light on the cause for the excess loss, because the input and output ports of the multiplexer are always looking into a 50-Ω characteristic impedance, within the bandwidth covered by the multiplexer (see Fig. 1).

The reason for this excess loss was traced to an effective detunning, relative to each other, of the filters in a given

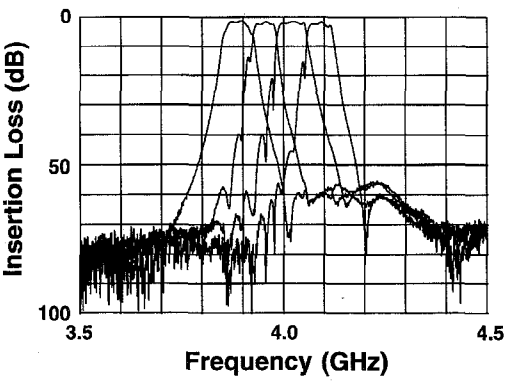


Fig. 7. Composite response of all four channels of the flight multiplexer.

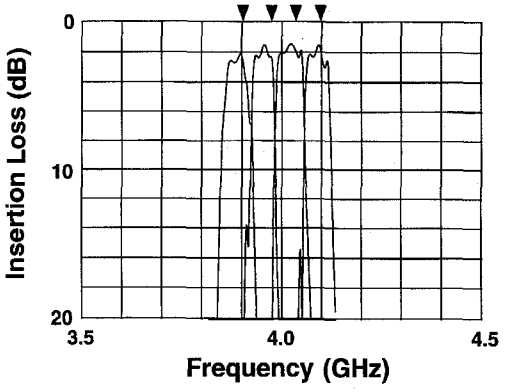
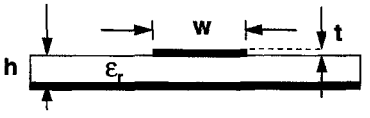


Fig. 8. Composite response of all four channels of the flight multiplexer, shown on an expanded 2 dB/div scale. The markers indicate the design center frequencies.

channel. Computer simulations using the ideal, lossless model of the channels, showed that center frequency offsets of 10 to 15 MHz are sufficient to produce an interference distortion in the passband. The resulting cancellation of energy yields a response that has a finite insertion loss which increases with the center frequency offset. This is shown in the series of plots in Fig. 9, made for different center frequency offsets between both filters in a channel. We conducted a systematic experimental and analytical search on the possible causes for this difference in center frequency between two filters in a channel. Table VIII shows the results of an analysis on the sensitivity of filter center frequency with respect to geometrical parameters and dielectric constant, assuming that only one at a time deviates from design. From Table VIII, a variation of 25 μm in substrate thickness causes a 5 MHz shift in center frequency, which is 10% of the design bandwidth (Table I). LAO substrate thickness was surveyed in our stock of both patterned and as yet unused wafers. It was found that the thickness was uniform to within 3 μm but that it was not uncommon to find substrates that were as much as 25 μm above or below the nominal 500 μm thickness. Although this is of serious concern in the future production of filters with accurate center frequencies, the substrate thickness nonuniformity was found to be too small to cause the shift in center frequency between the two filters on a channel.

The planar geometrical parameters, that is, the width and length of the resonators in a filter were found to require

TABLE VIII
SENSITIVITY ANALYSIS OF A MICROSTRIP HTS FILTER CENTER FREQUENCY VARIATIONS THE FILTER IS ASSUMED TO BE MADE UP OF RESONATORS WITH THE FOLLOWING CHARACTERISTICS: $f_o = 4$ GHz ($L = 1.001$ cm), $\varepsilon_r = 23.4$ (77 K), $h = 508$ μm, $w = 176$ μm, $t = 0.4$ μm



$\Delta\varepsilon_r$	Δh	Δw	ΔL	Δf_o
+0.1%	0	0	0	+2 MHz
0	+25 μm	0	0	+5 MHz
0	0	+10 μm	0	-5 MHz
0	0	0	+10 μm	-4 MHz

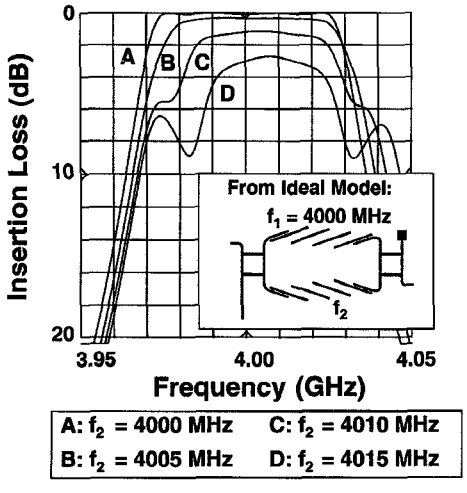


Fig. 9. Analysis from ideal channel model showing the effect of center frequency offsets between the two filters in a channel.

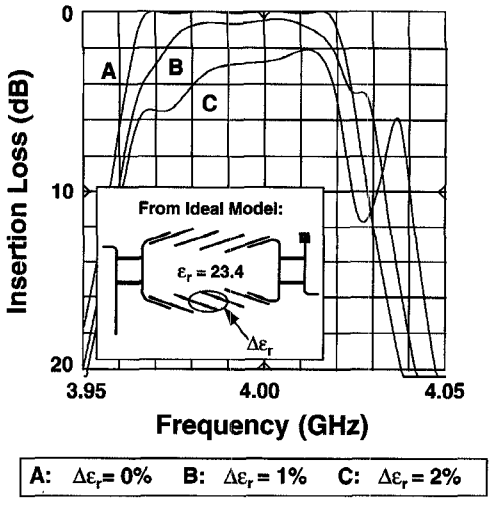
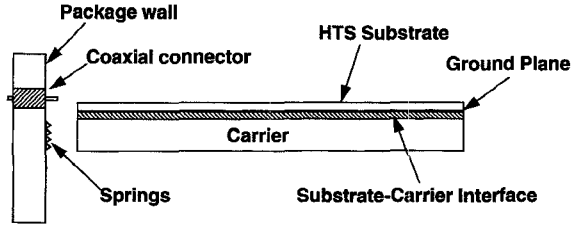


Fig. 10. Analysis from ideal channel model showing the effect of local changes in the substrate dielectric constant. This is a worst case where the change occurs in the weakest (most sensitive) coupled section.



Ground Return Path:

Ground Plane ⇨ Carrier ⇨ Springs ⇨ Coaxial Connector Outer Shield

Fig. 11. Schematic representation of the ground-current path. This diagram applies to both the HTS multiplexer and the delay line.

deviations from design that were too large to arise from tolerances in the standard photolithographic patterning process used to fabricate the filters.

As for the dielectric constant, Table VIII gives an idea of the effect of a change in ε_r from substrate to substrate. Because the single crystal LAO substrates show a twinning effect that might give rise to local nonuniformities in dielectric constant, this effect was considered further as a possible reason for filter-pair detunning in a channel. Fig. 10 summarizes the analysis conducted. A worst-case scenario was assumed in which deviations from nominal ε_r of 0, 1, and 2% were considered to occur in the weakest (and most sensitive) coupled section of the filter. It can be concluded from these plots that a significant alteration in the channel passband occurs for $\Delta\varepsilon_r$ between 1 and 2%. These are rather large values. Independent measurements of the relative dielectric constant nonuniformity in LAO substrates give values between 0.5 and 1% [19]. Nevertheless, this effect cannot be ruled out as yet and further research is needed in this area. It must be added that localized defects in the HTS films could cause the same effects as a local variation in dielectric constant.

Our experimental observations with a number of samples fabricated for this work support a different reason for the passband shapes and loss observed. We believe that the cause lies in the contact between the substrate ground plane and the package. Ground currents flow back to the coaxial connectors via the connection formed at the interface between the ground plane on the substrate and the carrier and then through the springs on the package frame. This is depicted schematically in Fig. 11. Our conclusion, from measurements after mounting and remounting several substrates patterned with multiplexer channels, is that the technique used to attach the substrates to the carriers in our packages, at the time this work was performed, needed further improvement to realize the full potential of High Temperature superconductivity. Spurious reactances caused by faulty ground contacts resulted in the somewhat degraded filter responses obtained.

III. DELAY LINES

A. Design

The design goals for the delay line are given in Table I. The final flight delay line unit delivered to the Navy was evolved from three delay line versions. All three designs were based on the same doubly-wound stripline spiral defined on a 5-

TABLE IX
PROCESS SEQUENCE FOR FINAL VERSION OF HTS DELAY LINE
SUBSTRATES ARE 5-CM-DIA., 250-μM-THICK $LaAlO_3$, WITH YBCO ON ONE SIDE

Mask	Description	Material	Thickness	Process
Bottom Wafer				
None	Ground plane contact	Au	2000 Å	Sputter
	Contact anneal	Au on YBCO	N/A	550°C
1B	Contact to YBCO spiral	Au	2000 Å	Lift-off
	Contact anneal	Au on YBCO	N/A	550°C
2B	Delay line spiral	YBCO	4000 Å	Ion mill
Top Wafer				
None	Ground plane contact	Au	2000 Å	Sputter
	Contact anneal	Au on YBCO	N/A	550°C
2T	Delay line spiral (image)	YBCO	4000 Å	Ion mill
3T/B	Ground plane openings	Au/YBCO	2000/4000 Å	Ion mill

cm-diameter, 250-μm-thick LAO wafer [14]. A discussion of why the stripline configuration was chosen over microstrip or coplanar waveguide is given in [14].

In all three versions, a -50 dB backward coupling between windings was used, corresponding to a spacing of 900 μm. The total delay on a 5-cm diameter wafer pair (stripline) was 22 ns, corresponding to a total delay line length of approximately 150 cm. The total required delay of greater than 40 ns was obtained by cascading two 22 ns delay line modules. Films on both surfaces of each LAO substrate were required in order to obtain the lowest insertion loss possible.

An initial version of the delay line was designed in which a 50-Ω line was defined on only one of the substrate surfaces that come in contact to form the stripline structure. Because of the high dielectric constant of LAO, a 50 Ω line is only 22 μm wide on 250-μm-thick substrates. This design was rejected early on because of practical difficulties in patterning such a long, narrow line without breaks due to film or fabrication defects.

A second version was then designed in which the line was widened to 150 μm (27 Ω) using 5-cm-long tapered impedance transformers at the input and output [20]. This solved the problem of low fabrication yield by making the line much less sensitive to small defects. Devices made with this design showed unacceptably high amplitude and phase ripple, however. The cause was traced to the effect of small air gaps between the contacting substrates making up the stripline structure. This effect was discussed in [14]. In order to avoid the deleterious effect of air gaps, mirror-image versions of the wider spirals described above were defined on both mating surfaces [20], [21]. Periodic contact between these two spirals then sufficed for good electrical characteristics. A short section of coplanar waveguide was inserted between the stripline and the coaxial connectors at the ends in order to facilitate the in-phase excitation of currents in both the upper and lower stripline ground planes and thus obtain good broad-band input/output matching [14].

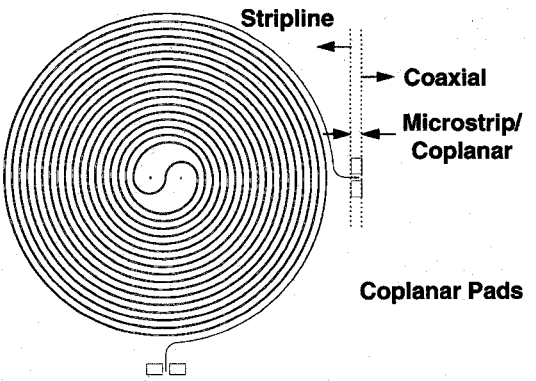


Fig. 12. Spiral stripline pattern for the bottom substrate of the HTS delay line.

B. Mask Layout and Fabrication

Fig. 12 shows the mask layout for the bottom wafer of a 22-ns delay line module [14]. Notice the coplanar transition and the taper from 22 μm (50 Ω) to 150 μm (27 Ω). The top wafer pattern is similar, but the spiral pattern begins after the impedance transformer in order to make alignment with the bottom wafer pattern less critical.

Processing of two wafers with YBCO on both sides was required, as summarized in Table IX. The bottom wafer had input and output contacts to its YBCO spiral, while the top wafer had no gold contacts. Both wafers had an annealed gold contact layer on the YBCO ground plane side. Processing was similar to that for the multiplexer discussed above.

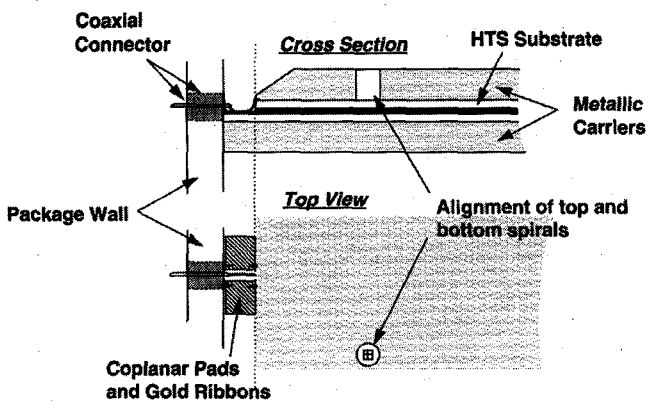


Fig. 13. Schematic diagram of the delay line coplanar transition and the alignment technique. For further details on the package refer to [14].

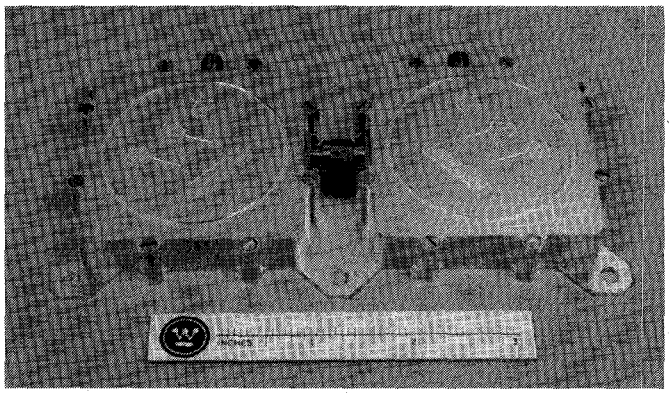


Fig. 14. Flight delay line package delivered to the Navy.

In order to align the mirror-image spiral patterns on top and bottom wafers during assembly, rectangular openings were milled into the ground plane of the top wafer opposite to alignment marks patterned on the spiral side. Since the LAO substrate is transparent, alignment marks on the fronts of the bottom and top wafers (i.e., the contacting surfaces) were visible through these rectangular openings on the ground plane, and matching openings in the top carrier, during delay line assembly. This is shown schematically in Fig. 13. Alignment of mirror-image spiral patterns will be discussed further in the next section.

The RF surface resistance at 77 K was measured for both sides of both wafers before fabrication began. The side with the lowest surface resistance was chosen as the spiral side.

C. Packaging and Assembly

Most of the packaging considerations applying to the filters also applied to the delay lines. But in contrast to the single-substrate microstrip filters, the stripline delay line required two contacting substrates for each device, half the thickness of those used for the multiplexer. An initial all-niobium package version was used for the early versions of the delay line design. However this package was upgraded to one similar to the final version of the multiplexer, using niobium only for the substrate carriers and aluminum for the frames with the connectors and for the lids. The carrier-substrate assemblies were also held on the aluminum frames by means of the same type of serrated springs attached to the frames.

Many of the packaging details used in the delay line were presented in [14]. A key feature of the package was the ability to accommodate and allow the alignment of the mirror-image spirals. The package incorporated a spiral spring contact around the periphery of the two substrates to make ground contact between the top and bottom carriers. The carriers were designed to allow slight differential lateral or rotational motion between upper and lower substrate-carrier assemblies, so that the contacting spirals could be brought into precise alignment. This was accomplished through the use of a fixture which produced the desired relative motion while fiducial marks on both substrates were brought into registration, as shown schematically in Fig. 13. The alignment was then held by casting molten bismuth-alloy solder into the interstitial space between alignment pins fastened to the bottom carrier and oversized alignment holes in the top carrier (see Fig. 4 of [14]). Pressure was applied by means of nuts and belleville washers on these pins.

The completed assembly was then inserted into the aluminum frame through which Wiltron K-connector glass-bead coaxial feed-throughs led the input and output from the delay line. As with the multiplexer, gap-welded gold ribbon was used to connect the coaxial center pin with the center strip line as well as the coplanar ground pads with the package structure. Fig. 13 shows schematically the transition from coaxial to stripline.

The final flight delay line delivered to the Navy consisted of two of the delay line packages described above, connected in series using male and female K-connectors and mounted on an aluminum plate with appropriate mounting holes. A photograph of the assembly is included in Fig. 14.

D. Experimental Results and Discussion

The measured performance of the flight HTS delay line at 77 K between 2 and 6 GHz is given in Fig. 15(a) and (b). There is a notch in the passband at about 5.8 GHz that was traced to a faulty ground plane contact between one of the substrates and its carrier. Similar notches were observed in later delay line samples that were corrected with reseating of the substrates on their carriers by heating up the assemblies.

Nevertheless, the amplitude ripple of this delay line was held to 1 dB or less as shown in Fig. 15(a). The ripple is mostly due to triple-transit between input and output connections. In order to make further improvements in the delay line performance, these transitions must be optimized. As with the multiplexer, ground current returns are of primary importance here as well. This involves both good quality, reliable, and repeatable ground contacting techniques and equalization of top and bottom ground plane current phases in the stripline portion of the delay line. Fig. 15(b) shows a measurement of delay, giving an average of 45 ns.

One of the modules used in the final delivery was tested up to 20 GHz [14], giving excellent performance and establishing the viability of building long delay lines (200 ns or more) using modules similar to these, for wide band applications.

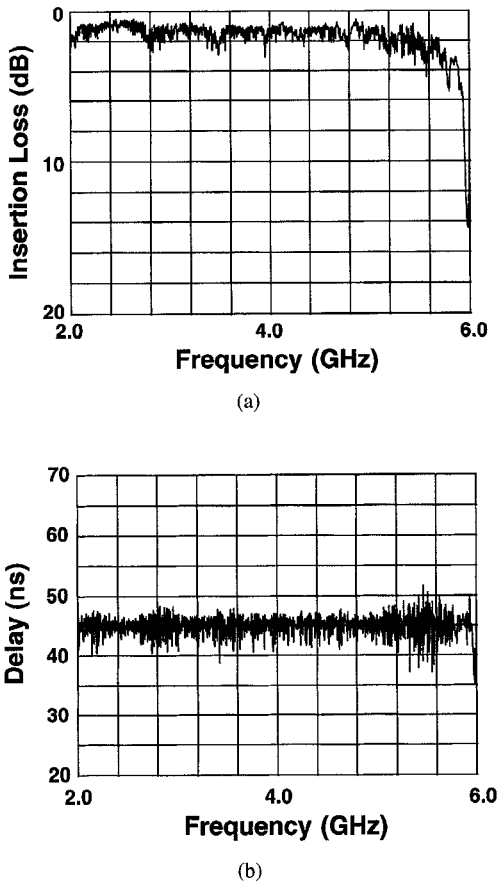


Fig. 15. Response of the flight HTS delay line between 2 GHz and 6 GHz at 10 dB/div scale (a) 2 dB/div scale. (b) Delay versus frequency.

IV. Conclusion

We have completed successfully the design, fabrication and space qualification of a high temperature superconducting four-channel multiplexer at 4 GHz and a 45 ns, 2-to-6-GHz delay line, both operating at 77 K. The space qualification of these devices was performed at the U.S. Naval Research Laboratory. This represents a milestone on the road toward practical, systems-qualified HTS microwave components. Many technological problems were solved in this effort and while many others remain, these two devices demonstrate the capability for design, fabrication and testing of high-performance, large-area HTS devices.

The ground plane contact between the substrate and the package was identified as a critical issue for obtaining desired loss and passband shape characteristics and will be the subject of future investigations for optimization.

Acknowledgment

The authors would like to thank Dr. R. S. Withers, Conductus, Inc., for bringing to their attention the deleterious effects of forward coupling caused by air gaps in stripline delay lines.

References

[1] A. Fathy, D. Kalokitis, V. Pendrick, E. Belohoubek, A. Pique, and M. Mathur, "Superconducting narrow band pass filters for advanced multiplexers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 1277–1280.

[2] R. R. Mansour, F. Rammo, and V. Dokas, "Design of hybrid-coupled multiplexers and diplexers using asymmetrical superconducting filters," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1993, pp. 1281–1284.

[3] R. R. Mansour, "Design of superconductive multiplexers using single-mode and dual-mode filters," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1411–1418, July 1994.

[4] R. R. Mansour, V. Dokas, G. Thomson, W. C. Tang, and C. M. Kudsia, "A C-band superconductive input multiplexer for communication satellites," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 12, pp. 2472–2479, Dec. 1994.

[5] R. R. Mansour, S. Ye, V. Dokas, B. Jolley, W. C. Tang, and C. M. Kudsia, "Design considerations of superconductive input multiplexers for satellite applications," *IEEE Trans. Microwave Theory Tech.*, P.E.: X-REF THIS ISSUE.

[6] R. S. Withers and R. W. Ralston, "Superconductive analog signal processing devices," *Proc. IEEE*, vol. 77, no. 8, pp. 1247–1263, Aug. 1989.

[7] Z.-Y. Shen, P. S. W. Pang, W. L. Holstein, C. Wilker, S. Dunn, D. W. Face, and D. B. Laubacher, "High Tc superconducting coplanar delay line with long delay and insertion loss," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 8, 1993, pp. 1235–123.

[8] G. C. Liang, R. S. Withers, B. F. Cole, S. M. Garrison, M. E. Johansson, W. S. Ruby, and W. G. Lyons, "High temperature superconducting delay lines and filters on sapphire and thinned LaAlO3 substrates," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 3037–3042, Sept. 1993.

[9] G. C. Liang, C-F Shih, R. S. Withers, B. F. Cole, M. E. Johansson, and L. P. Suppan, "Superconductive digital instantaneous frequency measurement subsystem," *IEEE Trans. Microwave Theory Tech.*, vol. 41, no. 12, pp. 2368–2375, Dec. 1993.

[10] N. Fenzi, D. Aidnik, D. Skoglund, and S. Rohlfing, "Development of high temperature superconducting 100 nanosecond delay line," *SPIE Proc. on High-Tc Microwave Superconduct. Applicat.*, vol. 2156, pp. 143–151.

[11] V. M. Hietala, J. S. Martens, T. A. Plut, C. P. Tigges, T. E. Zipperian, D. S. Ginley, and J. K. Truman, "High temperature superconducting slow-wave coplanar, transmission lines with normal-metal crossbars," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 6, pp. 972–975, Jun. 1994.

[12] M. Biehl, A. Vogt, R. Herwig, M. Neuhaus, E. Crocoll, R. Lochschmied, T. Scherer, W. Jutzi, H. Kratz, P. Berberich, and H. Kinder, "A 4-bit instantaneous frequency meter at 10 GHz with coplanar YBCO delay lines," *IEEE Trans. Appl. Superconduct.*, vol. 5, no. 2, pp. 2279–2282, Jun. 1995.

[13] S. H. Talisa, M. A. Janocko, D. L. Meier, C. Moskowitz, R. L. Grassel, J. Talvacchio, P. LePage, G. Hira, D. C. Buck, S. J. Pieseski, J. C. Brown, and G. R. Wagner, "High temperature superconducting four-channel filterbanks," *IEEE Trans. Appl. Superconduct.*, vol. 5, no. 2, pp. 2079–2082, June 1995.

[14] S. H. Talisa, M. A. Janocko, D. L. Meier, C. Moskowitz, R. L. Grassel, J. Talvacchio, P. LePage, D. C. Buck, R. S. Nye, S. J. Pi,eseski, and G. R. Wagner, "High temperature superconducting wide band delay lines," *IEEE Trans. Appl. Superconduct.*, vol. 5, no. 2, pp. 2291–2294, June 1995.

[15] S. H. Talisa, M. A. Janocko, C. Moskowitz, J. Talvacchio, J. F. Billing, R. Brown, D. C. Buck, C. K. Jones, B. R. McAvoy, G. R. Wagner, "Low- and high temperature superconducting microwave filters," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 9, pp. 1448–1454, Sept. 1991.

[16] S. H. Talisa, M. A. Janocko, C. K. Jones, B. R. McAvoy, J. Talvacchio, G. R. Wagner, C. Moskowitz, D. C. Buck, J. Billing, R. Brown, "Microwave superconducting filters," *IEEE Trans. Magn.*, vol. 27, no. 2, pp. 2544–2547, Mar. 1991.

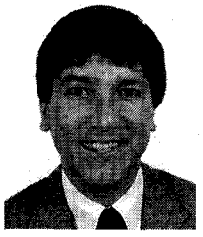
[17] J. W. Bandler, R. M. Biernacki, S. H. Chen, P. A. Grobelny, C. Moskowitz, and S. H. Talisa, "Electromagnetic design of high temperature superconducting microwave filters," in *IEEE Int. Microwave Symp. Dig.*, May 1994, pp. 993–996.

[18] R. C. Taber, "A parallel plate resonator technique for microwave loss measurements on superconductors," *Rev. Sci. Instrum.*, vol. 61, no. 8, pp. 2200–2206, Aug. 1990.

[19] M. L. Farich, S. H. Talisa, C. D. Cubbage, F. A. Miranda, and R Forse, "Measurement of LaAlO3 dielectric parameter variations," *1996 Appl. Superconduct. Conf.*, submitted.

[20] Dr. R. S. Withers, Conductus, Inc., private communication.

[21] G. L. Matthaei, and G. L. Hey-Shipton, "High temperature superconducting 8.45-GHz bandpass filter for the Deep Space Network," IEEE MTT-S Int. Microwave Symp. Dig., pp. 1273–1276, 1993.



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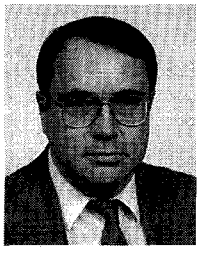

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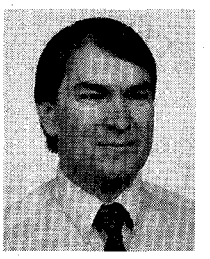
D. L. Meier, photograph and biography not available at the time of publication.



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Dr. Talvacchio is a member of the American Physical Society and the Materials Research Society.

C. Moskowitz, photograph and biography not available at the time of publication.

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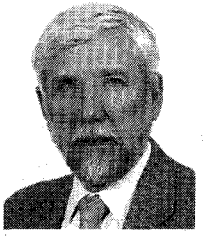
R. S. Nye, photograph and biography not available at the time of publication.

S. J. Pieseski, photograph and biography not available at the time of publication.



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